

ABSTRACT OF THE DISCLOSURE

An image processing apparatus includes a memory circuit, one-line judging circuit, a write control circuit and a read control circuit. The memory circuit stores an input data in response to a write address and outputs an output data in response to a read address. The one-line judging circuit receives a horizontal synchronization signal and a sampling clock signal and compares a number of pixels sampled within one line of the horizontal synchronization signal with a predetermined number so as to output a comparison signal and a difference signal representing a difference between the sampled number and a predetermined number. The write control circuit generates the write address in response to the clock signal and the comparison signal, and a read control signal in response to the comparison signal. The read control circuit generates the read address in response to the write address, the read control signal and the difference signal.